IN THE CLAIMS

1. (Currently Amended) A method of operating a non-volatile memory device driver comprising:

counting a number of write and/or erase access cycles to a non-volatile memory without regard to a failure of the write and/or erase access cycle; and

halting access to the non-volatile memory at a selected count.

2. (Original) The method of claim 1, wherein the driver is a low level driver.

3. (Cancelled)

4. (Cancelled)

5. (Original) The method of claim 1, further comprising:

restarting execution of the non-volatile memory command after halting execution at the selected count.

6. (Previously Presented) The method of claim 1, further comprising:

testing driver power loss recovery after halting access to the non-volatile memory at the selected count.

7. (Currently Amended) The method of claim 1, wherein halting access to the non-volatile memory at a selected count further comprises at a selected number of write and/or erase access cycles, counting the number of clock cycles and halting execution of the access cycle at a selected number of clock cycles.

8. (Original) The method of claim 7, wherein halting execution of the access cycle at a selected number of clock cycles further comprises removing power from the non-volatile memory.

9. (Original) The method of claim 7, wherein halting execution of the access cycle at a selected number of clock cycles further comprises loading an internal register in the non-volatile

memory and halting execution of a command execution logic of the non-volatile memory at the selected number of clock cycles.

10. (Original) The method of claim 7, wherein halting execution of the access cycle at a selected number of clock cycles further comprises loading an internal register in the non-volatile memory and halting execution of a command execution logic state machine of the non-volatile memory at a selected number of steps.

11. (Currently Amended) A method of operating a system comprising:

counting a number of write and/or erase access operations to a Flash memory device coupled to a host without regard to a failure of the write and/or erase access operations; and

stopping access execution to the Flash memory at a selected number of access operations.

12. (Cancelled)

13. (Original) The method of claim 11, further comprising:

examining a state of one or more host registers and/or the memory device after stopping execution.

14. (Previously Presented) The method of claim 11, further comprising:

rebooting the host after stopping access execution to the Flash memory.

15. (Original) The method of claim 11, further comprising:

executing power loss recovery routines on the Flash memory device.

16. (Currently Amended) The method of claim 11, wherein stopping access execution to the Flash memory at a selected number of write and/or erase access operations further comprises at a selected number of write and/or erase access operations, stopping execution of ~~the~~ a current write or erase access operation at a selected time period.

17. (Currently Amended) The method of claim 16, wherein stopping execution of the current write or erase access operation at a selected time period further comprises removing power from the Flash memory device.

18. (Currently Amended) The method of claim 16, wherein stopping execution of the current write or erase access operation at a selected time period further comprises loading an internal register in the Flash memory device with a selected number of clock cycles and halting execution of a command execution logic of the Flash memory device at the selected number of clock cycles.

19. (Original) The method of claim 16, wherein stopping execution of the access operation at a selected time period further comprises loading an internal register in the Flash memory device with a selected number of execution steps and halting execution of a command execution logic state machine of the Flash memory device at the selected number of steps.

20. (Currently Amended) A method of testing a Flash memory comprising:

counting a number of access operations to a Flash memory for a Flash command without regard to a failure of altering a state of any memory cell of the Flash memory altered by the access operations;

interrupting execution of the Flash command at a selected halt count of access operations, halting access to the Flash memory; and

executing a power loss recovery cycle to test power loss recovery at the selected halt count.

21. (Original) The method of claim 20, wherein counting the number of access operations further comprises counting a number of write and/or erase operations.

22. (Original) The method of claim 20, further comprising:

changing the selected halt count;

re-executing the Flash command;

counting a number of access operations; and

interrupting execution of the Flash command at the changed halt count.

23. (Original) The method of claim 22, wherein changing the selected halt count further comprises incrementing the selected halt count.

24. (Original) The method of claim 22, further comprising:

changing the Flash command after all possible halt counts of the Flash command have been tested.

25. (Previously Presented) The method of claim 20, wherein interrupting execution of the Flash command at a selected halt count of access operations, halting access to the Flash memory further comprises at a selected number of access operations, interrupting execution of the access operation at a selected number of clock cycles.

26. (Previously Presented) The method of claim 25, wherein interrupting execution of the access operation at a selected number of clock cycles, halting access to the Flash memory further comprises triggering external hardware to remove power from the Flash memory.

27. (Original) The method of claim 25, further comprising:

changing the selected number of clock cycles;

re-executing the Flash command;

counting a number of access operations to the selected access operation; and

interrupting execution of the Flash command at the changed selected number of clock cycles.

28. (Original) The method of claim 25, wherein changing the selected number of clock cycles further comprises incrementing the selected number of clock cycles.

29. (Previously Presented) The method of claim 25, wherein interrupting execution of the access operation at a selected number of clock cycles, halting access to the Flash memory

further comprises loading an internal register in the Flash memory with the selected number of clock cycles and halting execution of a command execution logic of the Flash memory at the selected number of clock cycles.

30. (Previously Presented) The method of claim 25, wherein interrupting execution of the access operation at a selected number of clock cycles, halting access to the Flash memory further comprises loading an internal register in the Flash memory device with a selected number of execution steps and halting execution of a command execution logic state machine of the Flash memory device at the selected number of steps.

31. (Currently Amended) A method of profiling a Flash command comprising:

counting a number of access operations to a Flash memory during execution of a Flash command without regard to a success or failure of the access operations to create an access operation profile for the Flash command; and

comparing the access operation profile of two or more Flash commands.

32. (Original) The method of claim 31, wherein counting the number of access operations further comprises counting the number of write and/or erase operations.

33. (Currently Amended) A system comprising:

at least one Flash memory device; and

a host coupled to the at least one Flash memory device, wherein the host is adapted to count a number of write and/or erase access operations to the at least one Flash memory device during a Flash command without regard to a success or failure of the write and/or erase access operations and halt execution of the Flash command, stopping access to the Flash memory device at a selected count of access operations.

34. (Cancelled)

35. (Original) The system of claim 33, wherein the at least one Flash memory device is one of a NAND Flash and a NOR Flash.

36. (Original) The system of claim 33, wherein an interface to the Flash memory device is one of a PCMCIA-ATA, a Compact Flash (CF), a USB Flash, MemoryStick, Secure Digital Memory Card, and a multimedia card (MMC) compatible interface.

37. (Original) The system of claim 33, wherein the host is one of a processor and an external memory controller.

38. (Currently Amended) The system of claim 33, wherein the host is adapted to count a number of write and/or erase access operations to the at least one Flash memory device during a Flash command and halt execution of the Flash command without regard to a success or failure of the write and/or erase access operations, stopping access to the Flash memory device at a selected count of write and/or erase access operations when a selected number of clock cycles has elapsed after issuing a last write or erase access operation that corresponds to the selected count of write and/or erase access operations.

39. (Currently Amended) The system of claim 38, wherein the system is adapted to halt execution of the last write and/or erase access operation at the selected number of cycles by removing power from the Flash memory.

40. (Currently Amended) A machine-usable medium, the machine-usable medium containing a software routine for causing a processor to execute a method, wherein the method comprises:

counting a number of write and/or erase access cycles to a Flash memory without reading any non-volatile memory cells written or erased by the write and/or erase access cycles; and

halting execution at a selected count of write and/or erase access cycles, halting access to the Flash memory.

41. (Cancelled)

42. (Currently Amended) The method of claim 40, wherein halting execution at a selected count, halting access to the Flash memory further comprises at a selected number of write and/or erase access cycles, counting the number of clock cycles and halting execution of ~~the~~ a current write or erase access cycle at a selected number of clock cycles.

43. (Currently Amended) A system comprising:

at least one Flash memory device; and

a host coupled to the at least one Flash memory device, wherein the host comprises a means for counting ~~the number~~ a number of write and/or erase access cycles to the at least one Flash memory device during execution of a Flash command without regard to a success or failure of the write and/or erase access cycles and comprises a means for halting execution of the Flash command on the at least one Flash memory device in response to the count of the access cycle counting means, stopping access to the Flash memory device.

44. (Currently Amended) The system of claim 43, wherein the host comprises a means for counting the number of write and/or erase access cycles to the at least one Flash memory device during execution of a Flash command and comprises a means for halting execution of the Flash command on the at least one Flash memory device in response to the count of the access cycle counting means, stopping access to the Flash memory device, when a means for timing the execution of a last write or erase access cycle has elapsed.